

## REMARKS/ARGUMENTS

Claims have been presented in a form which is believed to be more preferred by the Examiner and minor typographical errors have been corrected. A terminal disclaimer is hereby submitted herewith. Accordingly, it is respectfully requested that the Examiner withdraw the rejections under 35 U.S.C §101, 35 U.S.C §112, and Double Patenting.

In addition, independent claims have been amended to additionally recite the feature recited in claim 4. Claims have also been amended to further clarify that the reduced set of virtual machine instructions consists of a number of virtual machine instructions which is less than the number executable virtual machine instructions in a defined virtual machine instruction set (e.g., a conventional virtual machine instruction set).

The Examiner's rejection under 25 U.S.C § 102 over "Java Bytecode Compression for low-end embedded systems" ("*Clausen*") is fully traversed below.

It is noted that *Clausen* describes an algorithm for transforming a Java Bytecode program into an equivalent program factorized with respect to set patterns (*Clausen*, page 476). It is also noted that Fig. 4 of *Clausen* shows a factorized bytecode program along with a corresponding table of macros. However, it is respectfully submitted that *Clausen* does NOT teach or suggest selecting a first-reduced instruction from a reduced set of virtual machine instructions (claim 35). As noted above, *Clausen* teaches that a sequence of instructions can be replaced by a Macro instruction. However, it is respectfully submitted that *Clausen* does not teach or even remotely suggest: a reduced set of virtual machine instructions that provides substantially all of the functionality provided by defined virtual machine instruction set (e.g., a conventional virtual machine instruction set). Please note, for example, Appendix A of the present application which illustrates a mapping of a set of conventional Java Bytecode instructions to one or more instructions in a reduced set of virtual machine instructions provided in accordance with one embodiment of the invention.

Further, contrary to the Examiner's assertion, it is respectfully submitted that implementing an extensible JVM described in *Clausen* (section 5.1) does NOT teach

internally representing instructions as a pair of streams in a virtual machine (claim 36). Moreover, it is respectfully submitted that *Clausen* does NOT teach or even remotely suggest internally representing instructions selected from a reduced set of virtual machine instructions as a pair of streams.

Furthermore, contrary to the Examiner's assertion, it is respectfully submitted that *Clausen* does NOT teach determining whether a sequences of instructions selected from a reduced-set of instructions (i.e., a second sequence of bytecodes) includes a Getfield instruction immediately followed by an Astore instruction (claim 35).

Applicants hereby petition for an extension of time which may be required to maintain the pendency of this case, and any required fee for such extension or any further fee required in connection with the filing of this Amendment is to be charged to Deposit Account No. 500388 (Order No. SUN1P842). Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,

BEYER WEAVER & THOMAS, LLP



R. Mahboubian

Reg. No. 44,890

P.O. Box 70250  
Oakland, CA 94612-0250  
(650) 961-8300